CLAIMS

What is claimed is:

1. A system for synchronous communication between a first integrated circuit and a second integrated circuit comprising:

a synchronous interconnect structure for correcting timing alignment of a data signal and a source clock signal between said first integrated circuit and said second integrated circuit each time said data signal and said source clock signal are transmitted across said synchronous interconnect structure.

2. The system of claim 1, wherein said synchronous interconnect structure comprises, a deskewing circuit for connecting said timing alignment between said data signal and said source clock signal.

3. The system of claim 1, wherein said synchronous interconnect structure further comprises:

a transmitter circuit comprising a first transmitter and a second transmitter wherein said first transmitter asserts said source clock signal and said second transmitter asserts said data signal;

a receiver circuit comprising a first receiver and a second receiver wherein said first receiver receives said source clock signal asserted by said first transmitter and said second receiver receives said data signal asserted by said second transmitter; and

a first transmission line and a second transmission line, wherein said first transmission line interconnects said first transmitter and said first receiver

and said second transmission line interconnects said second transmitter and said second receiver.

4. The system of claim 3, wherein said first receiver and said second receiver each comprise a first receiver stage and a second receiver stage.

5. The system of claim 4, wherein said first receiver stage of said first receiver and said first receiver stage of said second receiver each comprise a signal conditioner to translate a received signal to a fixed output common-mode voltage.

6. The system of claim 4, wherein said second receiver stage of said first receiver and said second receiver stage of said second receiver comprises:

an integration sense amplifier to integrate and sense a value of said data signal after said correction of said timing alignment by said deskewing circuit.

7. The system of claim 2, wherein said deskewing circuit comprises:

a control circuit to control an amount of propagation delay inserted into a first transmission path within said deskewing circuit on which said data signal propagates and an amount of propagation delay inserted into a second transmission path within said deskewing circuit on which said source clock signal propagates, wherein the amount of propagation delay inserted into said first transmission path can have a value different from the amount of propagation delay inserted into said second transmission path; and

a phase-locked loop circuit to provide said control circuit with a output signal that indicates when the amount of said propagation delay should be inserted into said first and said second transmission path.

8. The system circuit of claim 7, wherein said control circuit comprises:

a detection circuit to determine and assert a correction signal if the amount of said propagation delay inserted into said first and said second transmission path needs adjustment; and

a delay circuit that inserts said propagation delay into said first and said second transmission path based on said input signal asserted by said phase-locked loop circuit and said correction signal asserted by said detection circuit.

9. The system of claim 8, wherein said detection circuit comprises:

a phase detector to detect a phase differential between said source clock signal and said data signal following the insertion of said propagation delay into said first and said second transmission path;

a counter to track the phase differential determined by said phase detector and assert said correction signal that indicates which direction said timing alignment should shift; and

a fault detector to detect when said data signal and said source clock signal toggle to allow said counter to track said phase differential when said data signal and said source clock signal both toggle.

10. The system of claim 8, wherein said delay circuit comprises,

a first delay element to insert said propagation delay into said first transmission path within said receiver;

a second delay element to insert said propagation delay into said second transmission path within said receiver; and

a finite state machine to interpret said correction signal asserted by said counter to control an amount of said propagation delay inserted into said first and second transmission path by said delay circuit.

11. The system of claim 7, wherein said phase-locked loop circuit comprises,

a voltage controlled oscillator (VCO) to generate said output signal, wherein said output signal has a frequency value proportional to a control voltage asserted at an input node of said voltage controlled oscillator;

a frequency multiplier to multiply the frequency value of said output signal asserted by the voltage controlled oscillator to provide said control circuit with a time varying signal synchronized to said source clock signal;

phase detector to detect a phase difference between said source clock signal and a feedback signal from said voltage controlled oscillator;

a charge pump to provide a charge current based on said phase difference detected by said phase detector; and

a loop filter to integrate and filter said charge current to drive said voltage controlled oscillator with said control voltage.

12. The system of claim 1, wherein said first integrated circuit and said second integrated circuit comprises a very large scale integration (VLSI) circuit.

13. The system of claim 1, wherein said first integrated circuit and said second integrated circuit comprises a microprocessor.

14. The system of claim 7, wherein said phase-locked loop circuit comprises a delay locked-loop circuit.

15. The system of claim 14, wherein said delay locked loop circuit comprises a voltage-controlled delay line (VCDL) to generate an output signal having a frequency value proportional to said control voltage asserted by said loop filter.

16. The system of claim 1, wherein said first integrated circuit and said second integrated circuit are mounted to a printed circuit board. (PCB).

17. The system of claim 1, wherein said first integrated circuit is mounted to a first circuit board and said second integrated circuit is mounted to a second printed circuit board.

18. A method for aligning a source clock signal and a data signal in a system having a synchronous interconnect structure between a first integrated circuit and a second integrated circuit while said synchronous interconnect structure transports data within said system, said method comprising the steps of receiving said source clock signal and said data signal at a receiver of said synchronous interconnect structure;

detecting a first phase offset between said source clock signal and a feedback signal at said receiver;

detecting a second phase offset between said source clock signal and said data signal at said receiver;

generating a time varying signal based on said first phase offset;

generating one or more delay values based on said second phase offset; and

adjusting in synchronization with said time varying signal a first propagation delay element within said receiver for said source clock signal and a second propagation delay element within said receiver for said data signal based on said one or more delay values to align a subsequent source clock signal and a subsequent data signal.

19. The method of claim 18, further comprising the step of, integrating said source clock signal and said data signal to determine a data value for said data signal.

20. The method of claim 18, wherein a delay-locked loop circuit within said receiver generates said time varying signal based on a value of said first phase offset.

21. The method of claim 18, wherein a counter circuit within said receiver generates a first of said one or more delay values based on a sampling of said second phase offset.

22. The method of claim 18, wherein a finite state machine performs said step of adjusting in synchronization with said time varying signal said first propagation delay element for said source clock signal and said second propagation delay element for

said data signal within said receiver based on said one or more delay values to align said source clock signal and said data signal.

23. The method of claim 18, wherein said first phase offset and said second phase offset are detected using a rising edge of said source clock signal and a rising edge of said data signal.

24. The method of claim 18, wherein said first phase offset and said second phase offset are detected using a falling edge of said source clock signal and a falling edge of said data signal.

25. The method of claim 18, wherein said first and said second propagation delay element comprise one of a phase interpolator and a transmission gate.

26. The method of claim 18, wherein said data signal comprises a differential signal.

27. The method of claim 18, wherein said synchronous interconnect structure comprises a multiprocessor interconnection network within said system.

28. A deskewing circuit to perform timing alignment of a synchronous point-to-point signal on a per signal basis comprising,

a control circuit to control said timing alignment of said synchronous point-to-point signal; and

a phase locked loop circuit to synchronize said timing alignment of said synchronous point-to-point signal within said control circuit.

29. The deskewing circuit of claim 28, wherein said control circuit comprises,

a detection circuit to detect a phase differential between a first data signal of said synchronous point-to-point signal and a source clock-signal of said synchronous point-to point signal; and

a delay circuit to perform said timing alignment of said first data signal and said source door signal based on an output signal of said detection circuit.

30. The deskewing circuit of claim 29, wherein said delay circuit performs said timing alignment by adjusting a first propagation delay circuit coupled to a first transmission path within said deskewing circuit by a first propagation delay value and adjusting a second propagation delay circuit coupled to a second transmission path within said deskewing circuit by a second propagation value, wherein said first transmission path transports said source clock signal and said second transmission path transports said first data signal.

31. The deskewing circuit of claim 29, said detection circuit comprising,

a counter circuit to count an occurrence of said phase differential and assert said output signal after a predetermined count; and

a fault detector circuit to detect a false count by said counter circuit, wherein upon detection of said false count said fault detector circuit instructs said counter circuit to disregard said false count.

32. The deskewing circuit of claim 28, wherein said phase locked loop circuit synchronizes said timing alignment by asserting a time dependent signal aligned to said source clock signal to synchronize operation of said delay circuit.